Process and device modelling for enhancement of silicon solar cell efficiency

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Abstract

Technology Computer-Aided Design (TCAD) using integrated process and device simulation tools is widely used in the semiconductor industry to reduce development costs and time, and to enhance device performance. In the PV industry, TCAD has usually focussed on device simulation. This paper shows results of integrated TCAD applied to the Laser Grooved Buried Contact (LGBC) silicon solar cell process, using 2D simulation of process steps to predict the solar cell structure and 2D device simulation of the resultant cell operation. This enables direct assessment of the impact of changing fabrication steps on key cell parameters such as V_{oc}, j_{sc}, FF and efficiency. Results suggest integrated TCAD may significantly accelerate development of future PV processes.

Introduction

TCAD is widely used in the microelectronics industry to reduce process development time and costs, and to ensure optimal performance of fabricated devices. In recent years TCAD models, especially those used to describe processing steps, have matured considerably as a result of hundreds of person-years of research in universities, institutes and companies (1). Process models now require relatively little 'calibration' to specific Si-based technology processes. At the same time, industry-standard device models have been extended to include opto-electronic interactions, thus enabling application to PV technology (2).

In the PV industry the use of TCAD is rapidly increasing, but is not yet well established. As in the microelectronics industry 1-2 decades ago the focus has mainly been on device modelling (3,4). Little if any work is done using integrated TCAD to investigate the impact of changes in processing steps. Such investigations are done using in-line processing experiments, despite difficulties in picking out true optima because of numerous trade-offs between process parameters, and variations arising from process fluctuations and drift.

In this paper, we explore the potential of integrated process and device modelling to optimise the processing of photovoltaic solar cells with respect to efficiency. By way of illustration we apply it to a well established technology, the LGBC solar cell manufactured by the New and Renewable Energy Centre (Narec). Process simulations are compared to short-loop process experiments, and then integrated process and device simulation is used to develop conclusions on trade-offs and potential further process optimisation of the LGBC process. Overall efficiency enhancements of at least 1% appear possible, even without back side passivation. Future papers will present the application of integrated TCAD to back side contacted, e.g. metal wrap-through (MWT) cells and alternative architectures.

Process modelling

The evolution of the wafer structure (a succession of doping processes, growth or deposition of layers, and layer removal) is modelled in 2D using a state of the art process simulation tool, Sentaurus Process. This tool uses advanced process models developed in collaboration with the nanoelectronics industry, institutes and universities. It also provides an interface for specifying custom models, and we use this to model the P surface concentration during the $POCl_3$ deposition process.

The wide range of length scales encompassed by a PV cell presents a significant challenge for process simulation. A manufactured cell usually has an area of 100 cm^2 or more, while the shallowest diffusions during processing can be less than 100 nm deep. In the simulations we take advantage of the repeating finger structure to model an 'elementary' cross-section through the cell, extending laterally from the mid-point between two fingers to the mid-point between the next two fingers, and vertically from the front to the back side of the wafer. However, even simulations using this smaller 2D 'simulation cell' are challenging, as the finite element grid spacing has to be as small as 10 nm in certain parts of the structure. For the purposes of process simulation, this remaining disparity of scales is handled by performing simulations in specific regions of the cell structure, and assembling them by spatial translation into the full simulation area to be used for device simulations. Key regions simulated are the shallow emitter, the corner regions of the groove structure, and the BSF doping. This assembly procedure may lead to slight errors in doping profiles, arising from neglect of long-range transport of point defects from areas of generation into adjacent regions (5).

However, in practice such errors are localised and (in this architecture) too small to affect device simulation results. Finally, in this work surface texturing used in manufactured cells is not explicitly modelled. This influences certain aspects of device simulation results, and where possible corrections to account for this will be discussed.

The initial step in the simulated LGBC process involves deposition of P, using a $POCl_3/O_2$ gas mixture. This step is modelled as follows. PSG is simulated as an oxide layer containing a high level of P, with calibrated interface states and diffusivity of P in oxide. The resultant trend in emitter sheet resistance versus deposition time is shown in Figure 1. Measured values (for consistency, obtained using non-textured wafers) are well described by the model simulations, and SIMS measurements of P emitter profiles (not shown) are also in reasonable agreement with simulations. The resulting calibrated model is expected to provide a fair basis for modelling the effects of different thermal cycles for the emitter diffusion.

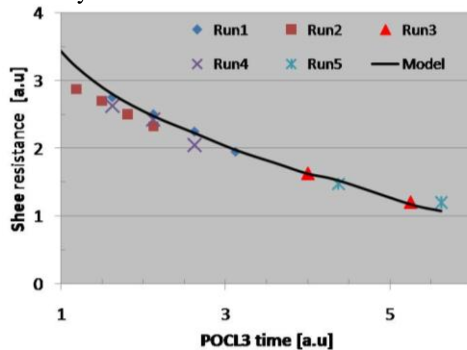

Figure 1: Experimentally measured and simulated emitter sheet resistance values after full high temperature treatment. Axis units are arbitrary units.

In the next simulation steps silicon nitride is deposited and part of the layered structure is removed to represent the laser cut groove structure. A further $POCl_3/O_2$ anneal at higher temperature is then simulated. This dopes the groove region with a heavier P concentration than was used for the shallow emitter. This completes the thermal processing steps for the front side of the wafer.

The following steps are used to model the formation of the back-surface field and the back contact. Al is deposited on the back side, and diffusion of Al atoms into the wafer is modelled assuming an Al-Si alloy has formed acting as a constant concentration diffusion source. The Al concentration on the silicon side of the alloy/silicon interface is set at the solid solubility limit for Al in silicon at the diffusion temperature. During cool-down from the peak set temperature, diffusion is neglected and the Al doping profile is assumed to be determined by epitaxial regrowth of Al-doped silicon following the thermodynamic equilibrium model derived and experimentally confirmed by Lölgen (6). The Al doping profile resulting from this thermal cycle is shown in Figure 2. It should be noted that this curve is an uncalibrated simulation and does not necessarily correspond to the true doping profile in the existing Al BSF process.

The proposal by Lölgen to incorporate B with Al for a higher concentration BSF (6) is modelled as an alternative process option. The model assumes that the thermodynamic properties of the liquid alloy are unaffected by the presence of B at the level of a few per cent, and that B is incorporated during regrowth at its solid solubility limit in silicon (an order of magnitude higher than that of Al). The result is of interest as this approach has not been widely used for BSF formation, although initial studies have shown promising results (7).

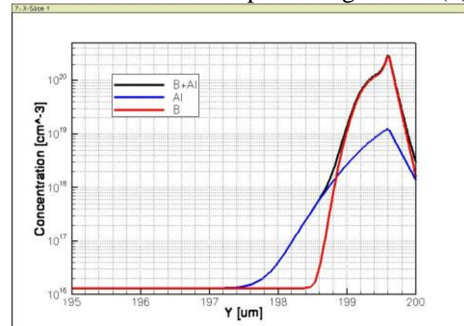

Figure 2: Simulated BSF doping profiles deposited using Al (existing process, blue curve), or Al:B alloy (black).

Device simulation

The full geometric structure used for device simulations, including the simulation grid, is shown in

Figure 3, together with details of the doping structure in the groove region. The overall structure is contacted along the back side of the wafer, and along the groove surface.

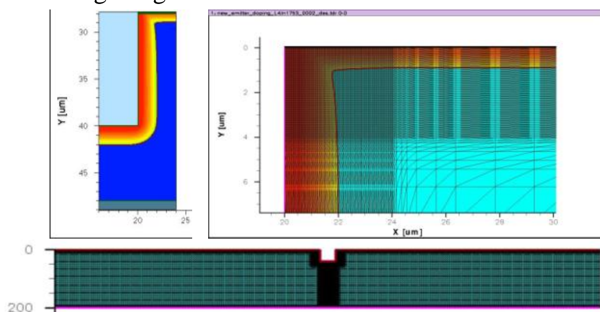

Figure 3: Geometry of simulated cell element. Details (at top) show the doping and mesh close to the groove. The emitter junction is marked by a solid line.

Simulations using Sentaurus Device are performed as follows. Reflection and transmission of light at material interfaces and light absorption in Si are calculated using the wavelength dependent complex refractive index of materials with the transfer matrix method (TMM). Electronic transport is simulated largely using default device models at 300K. Doping dependent recombination (SRH and Auger), carrier mobilities and bandgap narrowing are taken into account. The contact resistance of the groove finger is determined from room temperature measurements on fabricated cells with a range of dimensions. Finally the front

surface recombination velocity is set to 7500 cm/s. Bulk recombination at deep level centres is not considered as this is a material dependent issue. The lateral boundaries of the simulation are reflecting, thus correctly accounting for the repeated finger structure of a complete photovoltaic cell. Metal line resistance is neglected. Finally, for carrier generation the simulation assumes AM1.5 solar radiation incident normal to the cell surface.
Results for the potential distribution in the cell as it operates close to the maximum power point are shown in

Figure 4. The potential is near-constant in the wafer bulk and varies by <0.02V along the emitter. Potential changes larger than kT only exist in the vertical direction through the emitter/base junction and the BSF region, and where the emitter enters the groove region. Thus carriers are transported by diffusion in the bulk of the cell and within the emitter, and by drift/diffusion elsewhere.
A typical result for the total absolute current within the cell element is shown in Fig. 5. The main component of electron current flows almost directly upwards into the emitter and then along the emitter into the groove region, where it flows down around the groove, seeping into the groove contact at a rate limited locally by contact resistance. This final stage of current flow from the emitter into the groove contact is shown in Figure 6. By the time that the current reaches the bottom of the groove, most electrons have entered the metal, illustrating that the groove contact resistance does not significantly bottleneck the emitter current.
In addition to electron current arriving from the emitter, a smaller component of electron current (~1-3%, dependent on groove width and spacing) enters the groove directly from the base region. However, the impact of this current on the overall operation of the cell is quite small and the current flow in the base can be viewed as quasi one-dimensional, while the current flow in the emitter / groove region is inherently two-dimensional.

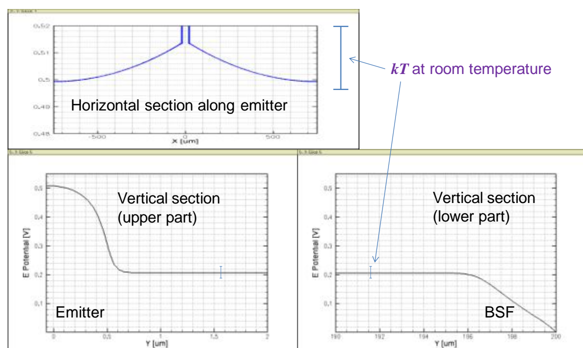

Figure 4: Electron potential distributions along sections through the simulation cell. Top: section along emitter below the silicon/oxide interface. Bottom: vertical section from emitter (left) to back surface (right).

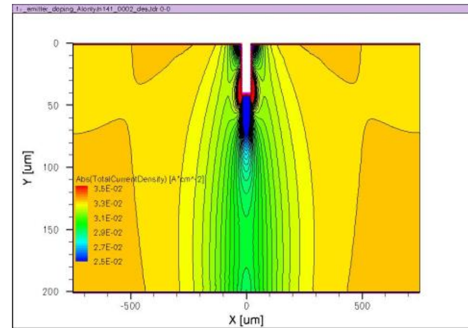

Figure 5: Simulation results for total absolute current in the full simulation element (for a 200μm-thick wafer)

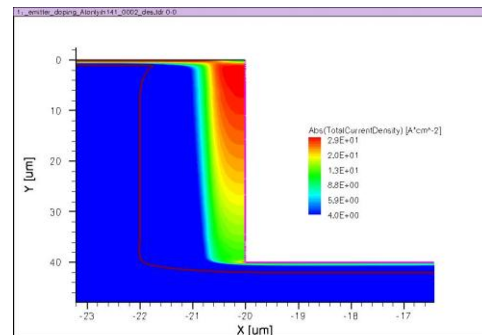

Figure 6: Current flow into the groove. Contact resistance causes current to enter the contact over an extended area. Note: X and Y scales are different.

Integrated simulations of the impact of processing on cell parameters

By sequentially running process and device simulations, the impact of a given series of process steps on cell parameters such as V_{OC}, I_{SC}, FF and efficiency can be evaluated. By varying the input process parameters, such as thermal anneal temperatures, deposition thicknesses, groove width and spacing, etc., a physically accurate picture of the process sensitivities of the cell technology can be constructed. This gives insight into the potential optimum efficiency of the process, how closely this efficiency has been approached in current manufacturing processes, and what steps may be taken to improve efficiency further.

Impact of cell geometry on efficiency

This section discusses the impact of groove spacing, groove width and wafer thickness on cell efficiency. Figure 7 shows the relative efficiency as a function of groove spacing. The optimal spacing is a trade-off between reducing shading and increasing the length –and hence resistance – of the emitter. The simulation is realistic for a planar surface but overestimates the optimal spacing in the textured case. This is because the emitter diffusion follows the topography of surface texture, leading to an increase in path length of electrons travelling along the emitter. Figure 8 shows the impact of groove width on efficiency. The results indicate a strong dependence arising from the fraction of cell area left uncovered by the groove.

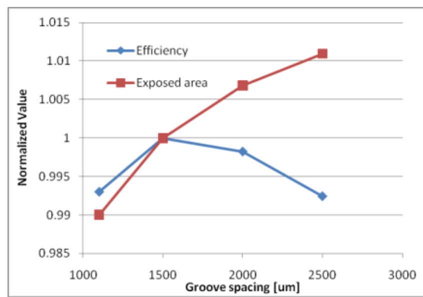

Figure 7: Efficiency as a function of groove spacing, calculated for a planar surface. At large spacing efficiency falls due to emitter resistance.

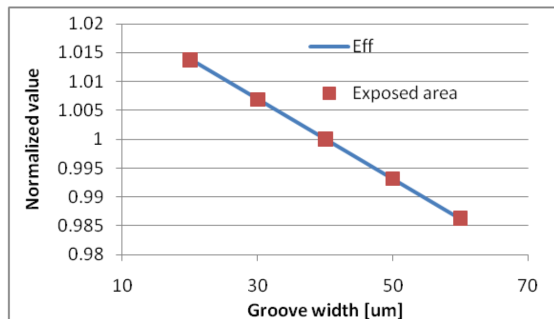

Figure 8: Dependence of relative efficiency on groove width, simulated for a non-textured cell

Figure 9 shows the efficiency as the wafer thickness varies. Thicker wafers result in higher efficiency because the total path length light can travel is increased.

Impact of doping processes on cell efficiency

The effects of modifications to the emitter and BSF doping processes have been evaluated in some detail. Efficiency at AM1.5 illumination is shown in Figure 10 as a function of P deposition time. This shows the benefit of a lightly doped, shallow emitter, if surface recombination is well controlled. Moving on to study the BSF, we show the potential impact of improved dopant profile engineering using Al:B co-doping. As illustrated in Figure 2, adding B to the BSF enables a peak p-type doping concentration > $10^{20}cm^{-3}$, an order of magnitude higher than with Al alone. The resulting decrease in back surface recombination strongly enhances device simulation results (Figure 11). Cell efficiency is substantially increased, and simulations also suggest a short post-anneal may increase the benefit from B doping. These results illustrate the cost effective way in which TCAD can help push the envelope of cell efficiency.

Conclusions

Integrated TCAD using physically accurate process and device simulation is applied to an established LGBC process and the operation of the resultant solar cells. Process variations are investigated in order to establish key technology issues and assess potential to improve this already well established technology. Although simulated efficiencies are not

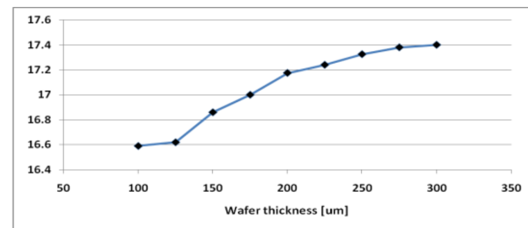

Figure 9: Efficiency as a function of wafer thickness.

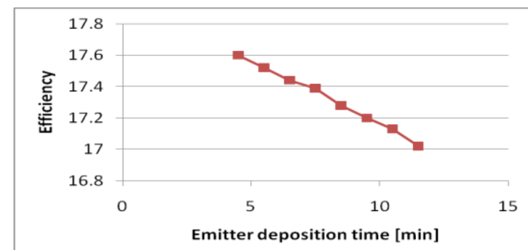

Figure 10: Efficiency versus emitter deposition time.

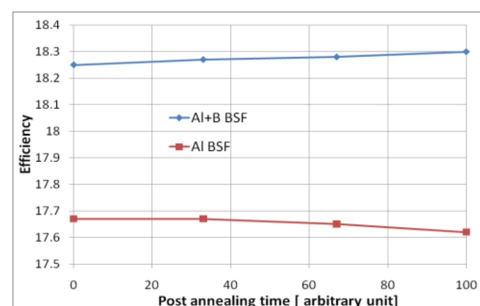

Figure 11: Efficiencies for the BSF doping conditions in Fig. 2. Adding B to the BSF appears to strongly increase efficiency. This may possibly be further improved using a short post-anneal.

precise absolute values, their variation shows important predictive trends. They can efficiently substitute for the extensive in-line experimentation and cell characterisation needed to obtain equivalent insights without simulation. Integrated TCAD – validated by small scale process experiments – is likely to become a regular feature of future efficiency improvement roadmaps in the PV industry.

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