INTEGRATED PROCESS AND DEVICE 'TCAD' FOR ENHANCEMENT OF C-SI SOLAR CELL EFFICIENCY

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ABSTRACT: Technology Computer-Aided Design (TCAD) using integrated process and device simulation is widely used in the semiconductor industry to reduce development costs and time, and to enhance device performance. In the PV industry up to now, TCAD has usually been limited to device simulation. This paper shows results of applying integrated TCAD using physics based simulation of process steps to predict the solar cell structure and 2D or 3D device simulation of the resultant cell operation. The approach is applied in detail to the simulation of Laser Grooved Buried Contact (LGBC) cells and initial results are also presented for Emitter Wrap Through and Metal Wrap Through (EWT/MWT) architectures. The use of integrated TCAD enables direct assessment of the impact of changing fabrication steps on key cell parameters such as V_{oc}, j_{sc}, FF and efficiency. Results suggest integrated TCAD will significantly accelerate development of future PV technology processes.
Keywords: Simulation, Manufacturing and Processing, c-Si

1 INTRODUCTION

Technology computer-aided design (TCAD) is a computer-based procedure that uses model representations of physical reality to predict (a) the device structures formed as a result of a specific chain of processing steps ('process simulation'), and (b) the electrical response of the resulting structure to boundary conditions such as contact potentials/currents and incident light ('device modelling'). TCAD is widely used in the microelectronics industry to reduce process development time and costs, and to ensure optimal performance of fabricated devices. In recent years TCAD models, especially those used to compute the effects of processing steps, have matured considerably as a result of hundreds of person-years of research in universities, institutes and companies (1). Two of the authors (CA and NEBC) have contributed significantly to this development. Process models now require relatively little 'calibration' to specific Si-based technology processes. At the same time, industry-standard device models have been extended to include opto-electronic interactions, thus enabling application to PV technology (2).

In the PV industry the use of TCAD is rapidly increasing, but is not yet well established. As in the microelectronics industry 1-2 decades ago the focus has mainly been on device modelling (3,4). Almost no work is currently done (as of 2010) to exploit integrated TCAD (process modelling input to device modelling) to investigate the impact of changes in processing steps on solar cell efficiency. Such investigations are done using in-line processing experiments and expert intuition, despite difficulties in picking out true optima because of numerous trade-offs between process parameters, and experimental fluctuations arising from processing variability and drift. This limited exploitation is surprising as integrated TCAD offers considerable opportunities to accelerate enhancements in cell efficiency, often at very little or even negative cost, and in future will undoubtedly impact strongly on industrial competitiveness, just as occurred historically in the semiconductor industry.

In this paper, we explore the potential of integrated process and device modelling to optimise the processing of photovoltaic solar cells with respect to efficiency. By way of illustration we apply it to a well established technology, the LGBC solar cell manufactured by the UK National Renewable Energy Centre (Narec). Process simulations are compared to short-loop process experiments, and then integrated process and device simulation is used to develop conclusions on trade-offs and potential further process optimisation of the LGBC process. Overall efficiency enhancements of at least 1% appear possible, even in this established process, and even without back side passivation. In the final technical section of the paper we outline the application of TCAD to emitter wrap-through (EMT) and metal wrap-through (MWT) cell architectures – these being current examples where TCAD can strongly accelerate the introduction and optimisation of higher efficiency solar cells from research and development to production.

2 APPLICATION OF INTEGRATED TCAD TO AN ESTABLISHED c-Si CELL TECHNOLOGY

2.1 Outline

Section 2 describes the application of TCAD to an existing c-Si technology process and the resulting fabricated solar cells. The procedure is similar to what is required to explore a novel technology, however it is easier to illustrate the impact of simulation by comparing to a known, well established technology. Section 3 takes a brief look at TCAD simulation for cell architectures that are currently being developed for production at a number of solar cell manufacturers.

The technology modeled in section 2 is the Laser Grooved Buried Contact (LGBC) solar cell process of the UK National Renewable Energy Centre in Blyth, UK. We first discuss the modeling of the fabrication process, and then use the resultant simulated structures as input information for device simulation of the operation of the fabricated solar cells.

2.2 Process modelling

The structure of the LGBC cell is well known, but for clarity in this discussion it is reproduced here, in Figure 1. The structure is processed to include a shallow emitter, passivation / antireflection coating, grooves, groove diffusion, Al back-surface field and contacts.

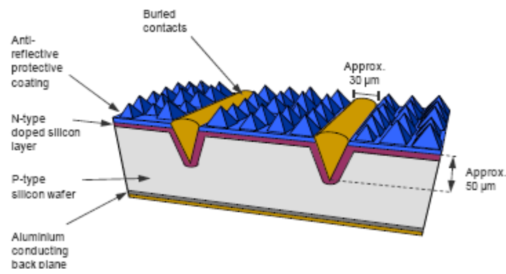

Figure 1: Schematic diagram of the LGBC solar cell structure

The evolution of the wafer structure (a succession of doping processes, growth or deposition of layers, and layer removal) has been modelled in 2D using a state of the art process simulation tool, Sentaurus Process. This tool uses advanced process models developed in collaboration with the nanoelectronics industry, institutes and universities. It also provides an interface for specifying custom physical models, by coding their mathematical formulation in a TCL based language. This is a valuable feature of the Sentaurus tool, which we use here for example to model the P surface concentration during the $POCl_3$ deposition process.

The wide range of length scales encompassed by a PV cell presents a significant challenge for process simulation. A manufactured cell usually has an area of 100 cm^2 or more, while the shallowest diffusions during processing can be less than 100 nm deep. In the simulations we take advantage of the repeating finger structure to model an 'elementary' cross-section through the cell, extending laterally from the mid-point between two fingers to the mid-point between the next two fingers, and vertically from the front to the back side of the wafer. However, even simulations using this smaller 2D 'simulation cell' are challenging, as the finite element grid spacing has to be as small as 10 nm in certain parts of the structure. For the purposes of process simulation this remaining disparity of scales is handled by performing simulations in specific regions of the cell structure, and assembling them by spatial translation into the full simulation area to be used for device simulations. Key regions simulated are the shallow emitter, the corner regions of the grooved finger structure, and the BSF doping. This assembly procedure may lead to slight errors in doping profiles, arising from neglect of long-range transport of point defects from areas of generation into adjacent regions (5), but in practice such errors are localised and (in this architecture) negligible. Finally, in this work, surface texturing used in manufactured cells is not explicitly modelled. This influences certain aspects of device simulation results, and where possible corrections to account for this will be discussed.

The initial step in the simulated LGBC process involves deposition of P, using a $POCl_3/O_2$ gas mixture. This step is modelled as follows. PSG is simulated as an oxide layer containing a high level of P, with calibrated interface states and diffusivity of P in oxide. The resultant trend in emitter sheet resistance versus deposition time is shown in Figure 2. Measured values (for consistency, obtained using planar non-textured wafers) are well described by the model simulations, and SIMS measurements of P emitter profiles (Figure 3) are also in reasonable agreement with simulations. The resulting calibrated model is expected to provide a fair basis for modelling the effects of different thermal cycles for the emitter diffusion.

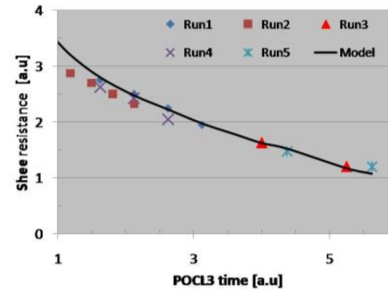

Figure 2: Experimentally measured and simulated emitter sheet resistance values after full high temperature treatment. Axis units are arbitrary.

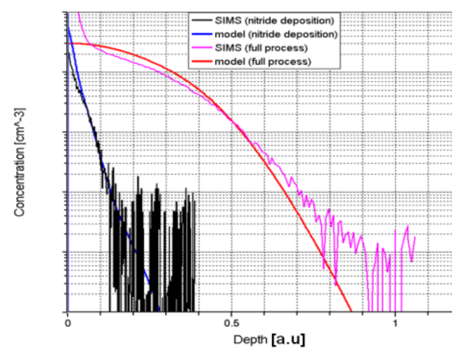

Figure 3: SIMS profiles and model simulations for the phosphorus (P) emitter profile after nitride deposition, and after a thermal budget equivalent to the full LGBC process sequence.

In the next simulation steps silicon nitride is deposited and part of the layered structure is removed to represent the laser cut groove structure. A further $POCl_3/O_2$ anneal at higher temperature is then simulated. This dopes the groove region with a heavier P concentration than was used for the shallow emitter. This completes the thermal processing steps for the front side of the wafer, however a further thermal budget is incurred as a result of the subsequent back surface field anneal, as described in further detail below. As a result the emitter profile broadens somewhat further and a deeper junction is also produced for the groove diffusion. Figure 4 shows the groove diffusion profiles obtained under the same annealing conditions as for the emitter diffusion in Fig. 3. The calibration established for the emitter diffusion works equally well in describing the groove diffusion profiles, without any need for adjustments.

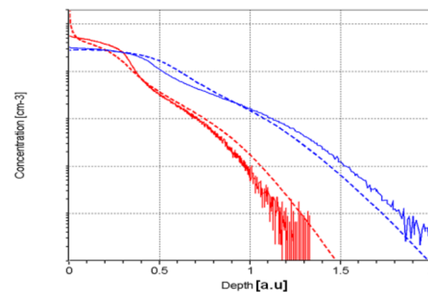

Figure 4: Experimental and simulated groove diffusion profiles, after nitride deposition and after the full LGBC process.

The following steps are used to model the formation of the back-surface field and the back contact. Al is deposited on the back side, and diffusion of Al atoms into the wafer is modelled assuming an Al-Si alloy has formed acting as a quasi 'constant concentration' diffusion source. The Al concentration on the silicon side of the alloy/silicon interface is set at the solid solubility limit for Al in silicon at the diffusion temperature. During cool-down from the peak set temperature, diffusion is neglected and the Al doping profile is assumed to be determined by epitaxial regrowth of Al-doped silicon following the thermodynamic equilibrium model derived and experimentally confirmed by Lölgen (6). The p-type doping profile resulting from this thermal cycle is shown in figure 5. It should be noted that this curve is an uncalibrated simulation and does not necessarily correspond to the true doping profile in the existing Al BSF process.

The proposal by Lölgen to incorporate B with Al for a higher concentration BSF (6) is modelled as an alternative process option. The model assumes that the thermodynamic properties of the liquid alloy are unaffected by the presence of B at the level of a few per cent, and that, with such B concentrations in the alloy, B is incorporated during regrowth at its solid solubility limit in silicon (an order of magnitude higher than that of Al). The result is of interest as this approach has not been widely used for BSF formation, although initial studies have shown promising results (7). We are currently planning physical experiments to test these predictions using cells to be processed on the Narec line.

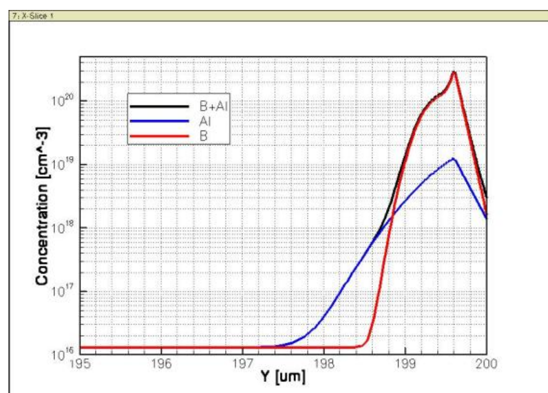

Figure 5: Simulated BSF doping profiles deposited using Al (existing process, blue curve), or Al:B alloy (black).

2.3 Device simulation

The full geometric structure used for device simulations of the LGBC cell, including the simulation grid, is shown in Figure 6, together with details of the doping structure in the groove region. The overall structure is contacted along the back side of the wafer, and along the groove surface.

Simulations using Sentaurus Device are performed as follows. Reflection and transmission of light at material interfaces and light absorption in Si are calculated using the wavelength dependent complex refractive index of materials with the transfer matrix method (TMM). Electronic transport is simulated largely using default device models at 300K. Doping dependent recombination (SRH and Auger), carrier mobilities and bandgap narrowing are taken into account. The contact resistance of the groove finger is determined from room temperature measurements on fabricated cells with a range of dimensions. The front surface recombination velocity is

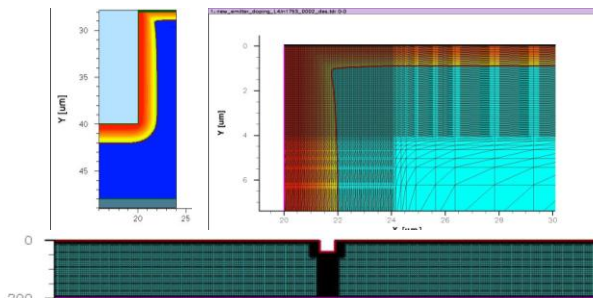

Figure 6: Geometry of simulated cell element. Details (at top) show the doping and mesh close to the groove. The emitter junction is marked by a solid line.

set to 7500 cm/s. Bulk recombination at deep level centres is not considered as this is a material dependent issue and is negligible in wafers with low levels of metal contamination after processing. The lateral boundaries of the simulation are reflecting, thus correctly accounting for the repeated finger structure of a complete photovoltaic cell. Metal line resistance is neglected to simplify the computation – including it requires the use of 3D simulation or 2D device simulation coupled to a transmission line circuit model, and does not further illuminate the trends to be discussed here. Finally, for carrier generation the simulation assumes AM1.5 solar radiation incident normal to the cell surface.

Results for the electrical potential distribution in the cell as it operates close to the maximum power point are shown in Figure 7. The potential is near-constant in the wafer bulk and varies by <0.02V along the emitter. Potential changes larger than kT only exist in the vertical direction through the emitter/base junction and the BSF region, and where the emitter enters the groove region. Thus carriers are transported by diffusion in the bulk of the cell and within the emitter, and by drift/diffusion elsewhere.

A typical result for the total absolute current within the cell element is shown in Figure 8. The main component of electron current flows almost directly upwards into the emitter and then along the emitter into the groove region, where it flows down around the groove, seeping into the groove contact at a rate limited locally by contact resistance. This final stage of current flow from the emitter into the groove contact is shown in Figure 9. By the time that the current reaches the bottom of the groove, most electrons have entered the metal, illustrating that the groove contact resistance does not significantly bottleneck the emitter current with the groove dimensions used.

In addition to electron current arriving from the emitter, a smaller component of electron current (about 1-3%, dependent on groove width and spacing) enters the groove directly from the base region. However, the impact of this current on the overall operation of the cell is quite small. Consequently the current flow in the base

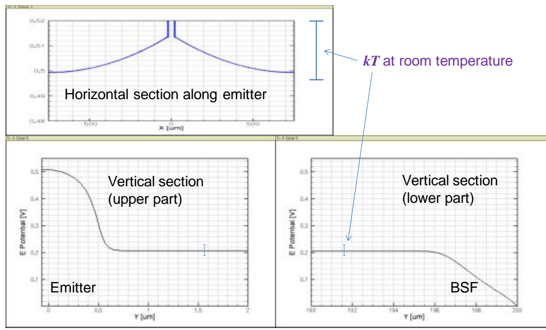

Figure 7: Electrical potential distributions along sections through the simulation cell. Top: section along emitter below the silicon/oxide interface. Bottom: vertical section from emitter (left) to back surface (right).

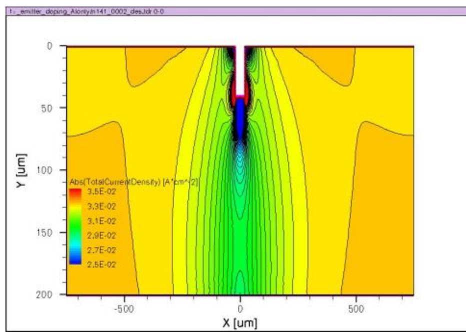

Figure 8: Simulation results for total absolute current in the full simulation unit cell (for a 200µm-thick wafer)

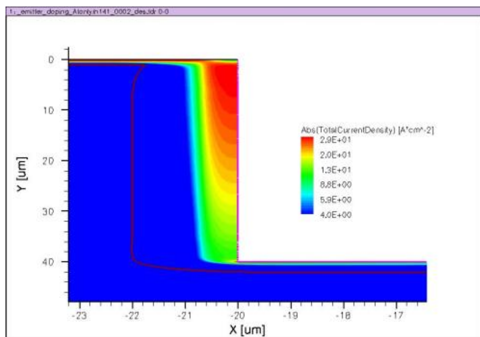

Figure 9: Current flow into the groove. Contact resistance causes current to enter the contact over an extended area. Note: X and Y scales are different.

can be viewed as quasi one-dimensional, while the current flow in the emitter / groove region is inherently two-dimensional.

2.3 Integrated simulations of the impact of processing on cell parameters

By sequentially running process and device simulations, the impact of a given series of process steps on cell parameters such as V_{OC}, I_{SC}, FF and efficiency can be evaluated. By varying the input process parameters, such as thermal anneal temperatures, deposition thicknesses, groove width and spacing, etc., a physically accurate picture of the process sensitivities of the cell technology can be constructed. This gives insight into the potential optimum efficiency of the process, how closely this efficiency has been approached in current manufacturing processes, and what steps may be taken to improve efficiency further.

In general this approach can be used to evaluate both the impact of cell geometry and the impact of altering processing steps on cell performance. Here we focus on the impact of changes in processing steps. The effects of modifications to the emitter and BSF doping processes have been evaluated in some detail. Efficiency at AM1.5 illumination is shown in Figure 10 as a function of P (n-type) emitter deposition time. This shows the benefit of a lightly doped, shallow emitter, if surface recombination is well controlled.

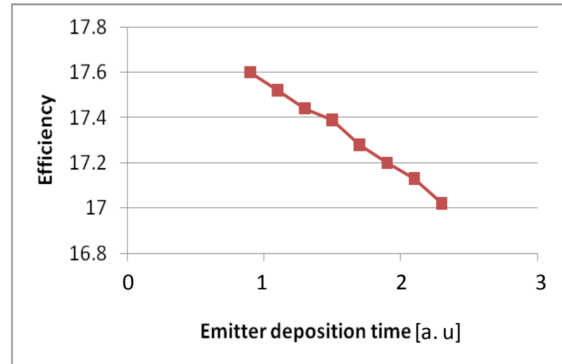

Figure 10: Simulated efficiency of the final fabricated cell, plotted versus the duration of the emitter deposition anneal.

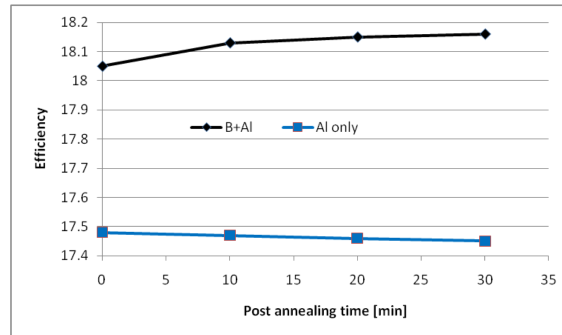

Figure 11: Simulated efficiencies for the BSF doping conditions in Figure 5. Adding B to the Al BSF appears to strongly increase efficiency. This may possibly be further improved using a post anneal.

Moving on to study the BSF, we show the potential impact of improved dopant profile engineering using Al:B co-doping. As illustrated in figure 5, adding B to the BSF enables a peak p-type doping concentration > 10^{20}cm^{-3}, an order of magnitude higher than with Al alone. The resulting decrease in back surface recombination strongly enhances the cell efficiency predicted by device simulation (Figure 11).

Integrated simulations also suggest that post-annealing may increase the benefit from B doping. These results illustrate the cost effective way in which TCAD can help push the envelope of cell efficiency, even for a process that is well established and appears to be already fully optimized.

3 TCAD SIMULATION OF EMITTER WRAP-THROUGH BASED ARCHITECTURES

3.1 Outline

This section briefly illustrates the use of 3D TCAD simulations for prediction of cell performance in advanced c-Si cell architectures. A first discussion of EWT cell operation supported by 3D TCAD analysis gave insight into via resistance effects in the EWT cell [8]. In this work we illustrate the application of 3D TCAD to evaluate trends in cell efficiency as functions of cell geometry and via processing (EWT versus MWT).

3.2 Geometry, illumination and current distributions

The schematic structure of the EWT unit cell surrounding a single wrap-through cylindrical 'via' is shown in figure 12.

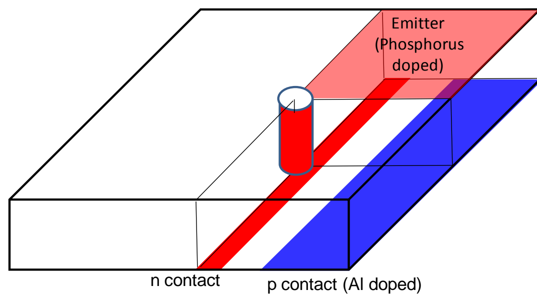

Figure 12: Schematic of emitter wrap through structure showing unit cell around a single via.

In the following 3D figures the same basic structure, used in our numerical simulations, is presented. The unit-cell structure is inverted to show the back side contacts. The simulation assumes a square array of via holes, and thus by symmetry the unit cell can be represented conveniently using one quarter of the volume surrounding a single via of radius *r*. This region is simulated using ~10^6 finite elements, leading to random-access memory requirements for efficient simulation of ~10^{10} byte. Typical cpu times on a PC based processor cluster with sufficient available memory are a few times 10^5 s for a single I-V characteristic. Figure 13 shows the basic structure, with contacts removed from the visualization for clarity. The emitter doping is shown in red and the base doping in blue.

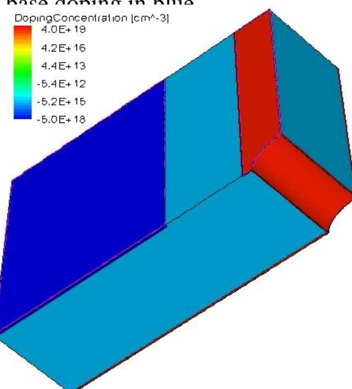

Figure 13: Quarter unit-cell of the EWT structure, inverted to show the back side contacts.

Figures 14 to 17 show the simulated optical carrier generation, total current density, hole current density, and electron current density in the cell.

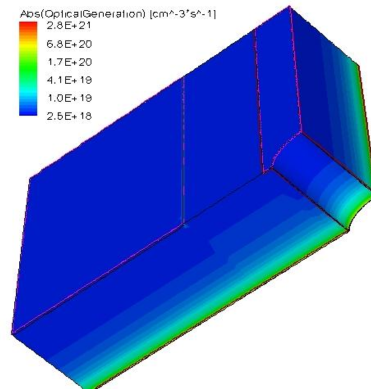

Figure 14: Simulated optical generation in the EWT cell

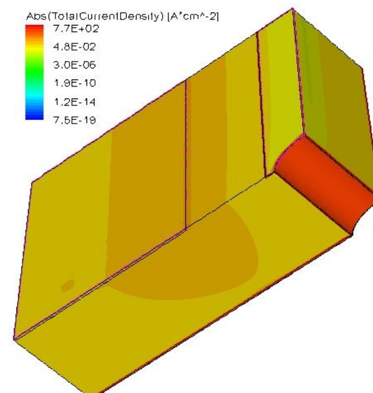

Figure 15: Simulated total current density in the cell

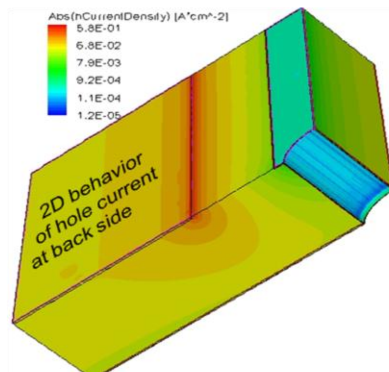

Figure 16: Simulated hole current density in the cell

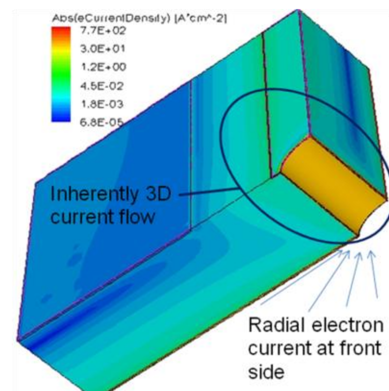

Figure 17: Simulated electron current density

Owing to the geometry the current flow in the top side emitter region is approximately radial (electrons flowing towards the via) while that in the back side region is approximately Cartesian (holes flowing towards the base contact and electrons flowing towards the back side emitter contact). In the region around the via, current flow is fully 3-dimensional, with a quasi 1D current of electrons flowing from the front side emitter to the back side and more complex flows of electrons and holes in the surroundings of the via. Efficiency can be significantly limited by the rate of flow of electrons along the via to the back contact.

3.3 Efficiency as function of cell geometry and via processing

Figure 18 shows the dependence of efficiency on via radius for the case of (a) emitter wrap-through technology where electron current along the via passes through the surrounding emitter doping, and (b) metal wrap-through technology where the hole is filled with metal. In the metal wrap-through case we have assumed the limiting case where the metal acts as a perfectly conducting contact with no break of continuity. As expected, in the emitter wrap-through case (without metal fill), efficiency peaks at an intermediate via radius, found here to be ~20 μm, while in the metal wrap-through case, efficiency rises towards even smaller via radii. The optimal radius is determined by a trade-off between via resistance and optical shadowing, and depends on the emitter doping characteristics. A detailed analysis of this problem, taking into account the details of alternative emitter doping processes, will be presented in a forthcoming paper.

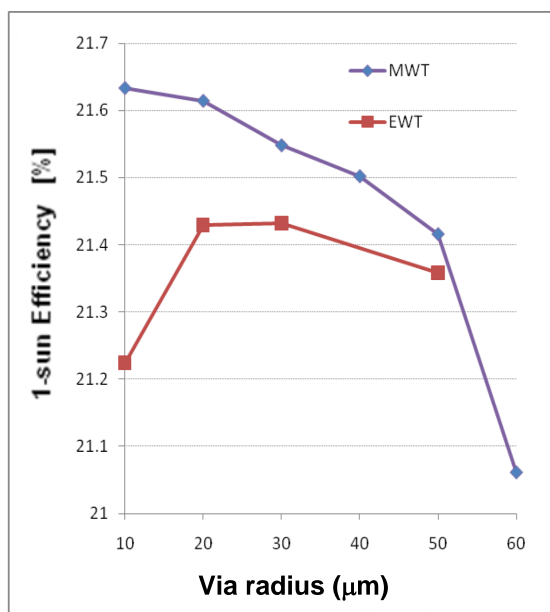

Figure 18: Efficiency as a function of via radius for the EWT and the MWT. The EWT efficiency peaks at an intermediate value ~20 μm due to a trade-off between shadowing and via resistance. The efficiency for the MWT case (assuming perfectly conductive metal fill) continues to increase towards smaller via radii.

4 SUMMARY AND CONCLUSIONS

Integrated TCAD using physically accurate process and device simulation has been applied to predict the structure and operation of c-Si solar cells. Predictions for the established LGBC process are in good agreement with observed trends of efficiency as a function of processing conditions. Moreover we have predicted further improvements that could potentially be made to the LGBC process, even though this is a well established technology which had appeared to be already optimized. This makes clear that, while experimentation is always required, integrated TCAD can efficiently substit ute for the very extensive in-line experiments and cell characterisation studies needed to obtain equivalent insights without simulation.

TCAD simulations for more advanced c-Si architectures – emitter wrap-through and metal wrap-through – have been performed in 3D to assess the impact of metal filling and study the dependence of efficiency on via radius. This approach is likely to support a significantly faster development of advanced c-Si PV technologies from the imagination of the inventor, through the laboratory scale into production. One can foresee that integrated TCAD – always validated by process experiments – may become a critical component of future efficiency improvement roadmaps in the PV industry.

ACKNOWLEDGEMENTS

We would like to thank Georgoe Letay for advice on the use of Sentaurus Device for optics simulations.

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