Investigation of Cross Wafer Uniformity of Production-Line-Produced LGBC Concentrator Solar Cells

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Introduction

At NaREC, the Laser Grooved Buried Contact (LGBC) technology, shown schematically in cross section in figure 1, is utilised to produce both multi and mono crystalline silicon solar cells [1].

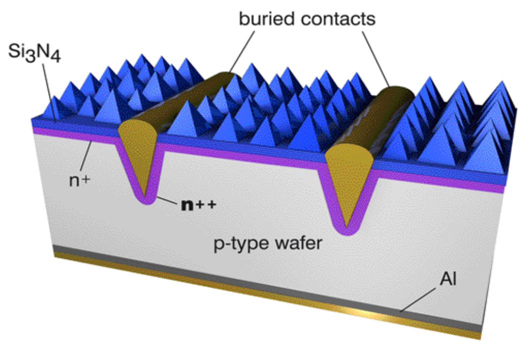


Fig.1. Schematic of LGBC solar cell.

One NaREC speciality is the volume fabrication of silicon concentrator photovoltaic (CPV) cells for operation up to 100x concentration. For these devices many individual cells are manufactured on a single wafer. For these applications, spatial uniformity across all processing steps is important to maintain homogeneous cell performance across the wafer.

This paper illustrates the results from some of the techniques used to characterise the uniformities within the thermal processing steps of the LGBC production line. Investigations were carried out to establish how these spatial profiles subsequently relate to cell performance and efficiency.

Initial work centred on the groove diffusion (GD) furnace process, used to produce selective doping in the grooved region of the silicon to optimise the metal contact resistance. The success of this process is crucial to the subsequent electroless plating steps. Detailed understanding of the groove diffusion wafer sheet resistivity uniformity was established and source of variation (SOV) studies carried out to ascertain the main contributors to total doping variation within the furnace step. Run-by-Run analysis was completed over several months to establish first stage statistical process controls (SPC) to maintain long term process stability.

Processing Equipment

NaREC's GD processing is performed under high temperature in an atmospheric pressure chemical vapour deposition (APCVD) horizontal tube furnace as shown in figure 2. The step involves controlled phosphorus doping of the cell surface. Wafers are placed in slots within a quartz boat in an orientation such that only the front surface receives doping.

Fig.2. NaREC's Centrotherm horizontal furnace

Measurement technique

To gauge the success of the doping process, monitor test wafers are placed within the production run. These wafers are given the standard pre clean, furnace processing and then post clean steps along with the production wafers. Once post clean is completed, the monitor wafers are measured for sheet resistivity on a contact 4 point probe in the standard method as previously presented [2]. A higher doping level results in a lower sheet resistivity.

Measurement Sample plan per wafer

To ascertain a suitable quantity of data points from each wafer in the study, a very high site count wafer was measured (> 45 sites). By mapping the results of this and several other processed test wafers, a repeatable spatial pattern was observed. The results consistently showed a ring effect of higher doping levels around the edge of the wafer with an oval of least doping just above the centre of the wafer. The results range was only in the order of 5 ohm/sq. This spatial signature is shown in the map in figure 3.

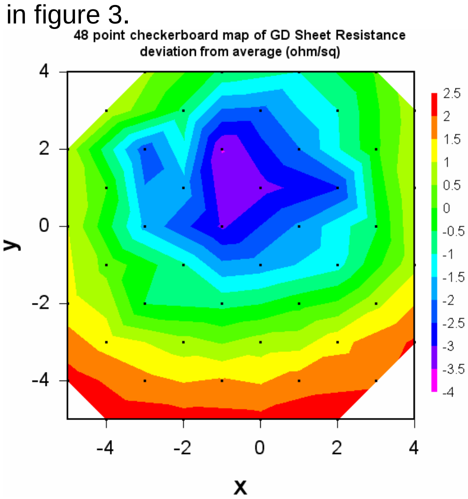


Fig.3. Schematic of results for Checkerboard Sample plan

A cross-shaped sample plan as shown in figure 4 was adopted to capture this repetitive signature in subsequent processing runs.

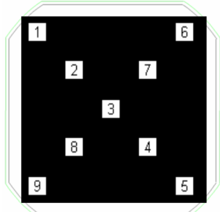


Fig.4. Adopted 9 point-sample plan

Source of Variation Study

Using the new sample plan, multiple test wafers were inserted at various places within a production run. In this run, only 2 out of the available 5 quartz boats were required for production as described in Appendix 1. This study therefore evaluated variations due to slot position, facial direction, site-within-boat, boat position and site-on-wafer in these two boats. A close-up schematic of the test wafer plan for Boat 2 and 3 can be seen in figure 5.

Source of Variation Results

Every test wafer was measured in accordance with the 9 point sample plan. This raw data was then analysed in reference to the corresponding locations within the furnace. Firstly, the 9 raw data points per wafer were graphed with reference to the quartz boat and slot location used (ref. figure 5) as well as facial direction.

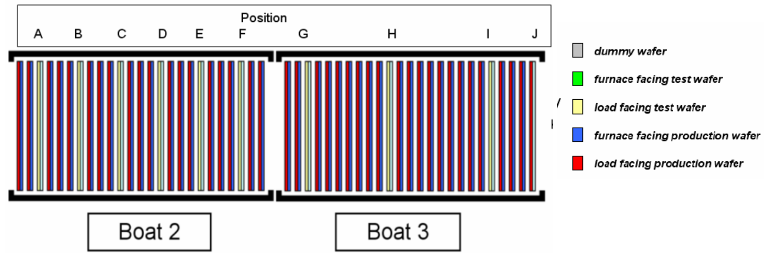


Fig.5 Experiment layout of Boat 2 and 3

The 171 data points when plotted by boat number, position-within-boat and facial direction (facing towards loader or oven/gas side of furnace) show a common spread of results with only the wafer in position J showing a tighter distribution as seen in figure 6. Wafer J has a special assignable cause to explain its behaviour as it is placed next to a dummy wafer in the furnace. It will be screened from further analysis as we concentrate on the investigation of common variation causes.

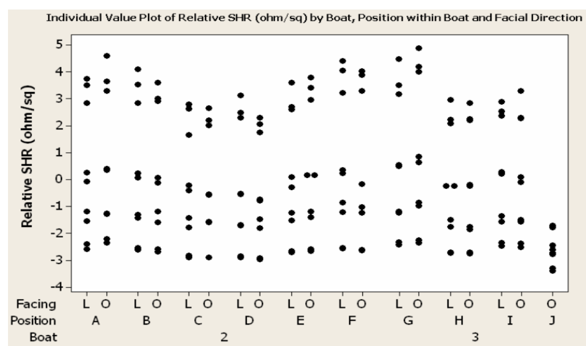


Figure 6. Sheet resistance data by position in furnace

By choosing a different analysis technique for the same data, a better picture can be seen of the different sources of the variation in sheet resistance. By grouping the data by each individual contributor and comparing the mean (average) of the different groups, the variation due to differences in the groups is established as displayed in Figure 7. The contribution to the variation from the facial direction, the boat position, the slot and position within the boat are not significant to the total variation. This is illustrated by only small differences in the means of their data results. However, the plot that relates to the site position on the wafer shows significant differences between the mean of the groups.

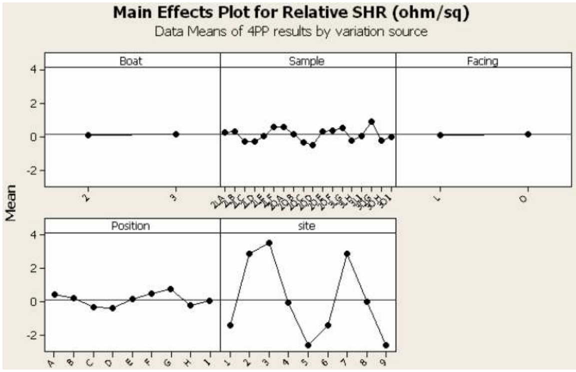


Figure 7. Mean effects plot for Sheet resistance.

The 9 sites correspond to the sample plan illustrated in figure 4. This can be demonstrated further by displaying the results data by site as in figure 8.

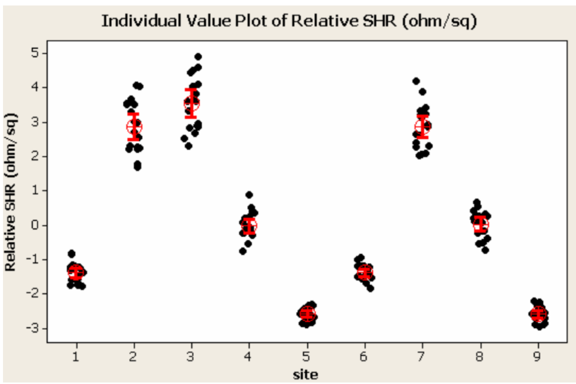


Figure 8. Relative sheet resistance data by site

It is possible therefore to predict the value of the sheet resistance of the test wafer in the furnace based only on its wafer site location. The major source of variation in this process is site-to-site variation i.e. cross wafer uniformity. Therefore for ongoing process monitoring a sample of a single wafer per run with measurement of 9 sites per wafer is sufficient to capture the range of variation in the run.

Ongoing monitoring

A run-by-run check was implemented and data gathered and monitored over time. Once 20 runs had been completed a stability assessment was made on the behaviour of the process. The distribution of the mean, median and range data proved the data was behaving in a normal distribution suggesting process stability. These graphs are shown in figure 9. Plotting the 20 run data using statistical process control (SPC) charting gave a stability control limits for both the mean and the range results.

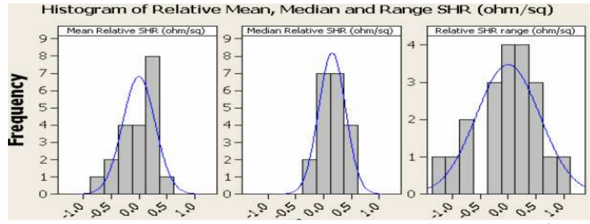


Figure 9. Histogram summaries of SHR results from first 20 GD runs

The techniques and statistical tests used here utilise the Western Electric standards [3]. These controls were implemented into production to provide a monitor for the process stability over time. The target value was set based on the mean of the first 20 runs and the upper and lower control limits set to $\pm$ 3 standard deviations of the distribution of the first 20 runs as displayed in figure 10.

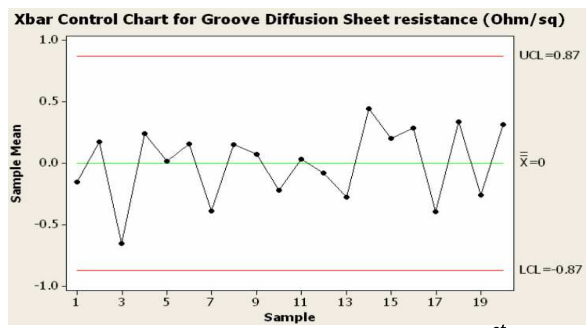


Figure 10. Derived control limits from 1st 20 GD runs

This data collection was continued over several more months and data tested continuously for stability within the original limits. Good statistically stable behaviour was demonstrated over this time with no data point behaving in a non-random fashion i.e. all points are within statistical control. The results from the 1st 40 runs are shown in figure 11.

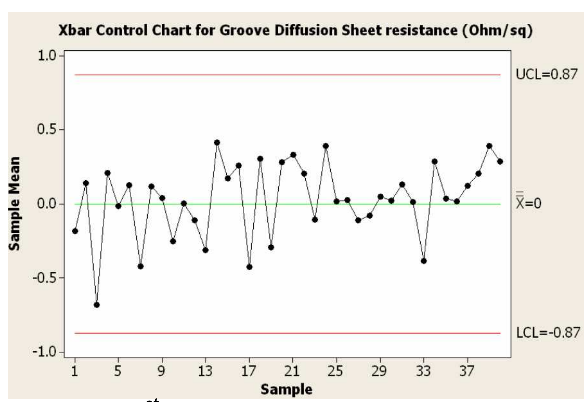


Figure 11.1st 40 GD runs tested against original control limits.

Effect of GD uniformity on solar cell performance

To assess the effect of the GD doping uniformity, a trial was run using a proprietary CPV cell that has 36 cells within a single 12.5cm pseudo square wafer. The wafers were monitored through the groove diffusion process steps for the standard sources of variation e.g. orientation and placement within boat. Once completed the individual cells were measured at 1SUN levels and the performance of the cells compared in reference to their position within the GD furnace and within the wafer as described in figure 12.

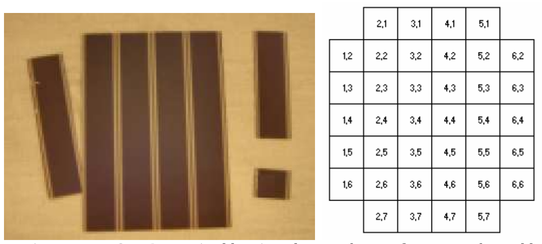


Figure 12. Partially isolated wafer and cell labeling convention for analysis

The results, shown in figure 13, indicate a slight spatial dependence upon location within wafer. However, this dependence had a comparable level to the dependence upon wafer itself so is not a dominant factor. Also, when mapped, this dependence does not coincide with our earlier observations with regard to GD doping across a wafer which showed a non-centred cross wafer signature. So while there is a centre-to-edge profile for our cell parametrics, these are unlikely to be caused by the GD process itself. The cell efficiency is plotted by location on wafer of the cell in figure 14.

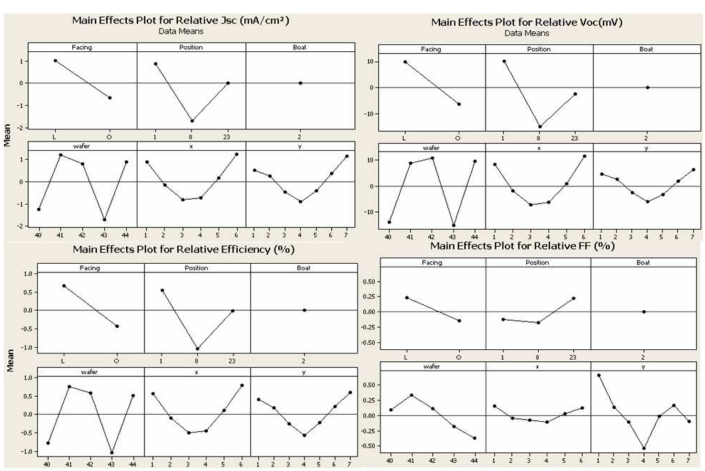


Figure 13.Main-effects plots for 1 SUN Cell test

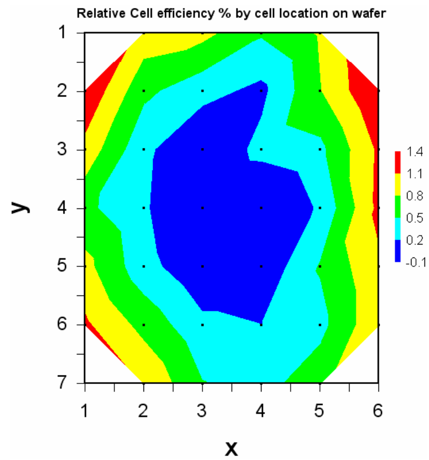


Figure 14.Sample of Efficiency plotted by location

Conclusions

NaREC has a very stable APCVD process for its Groove Diffusion step. Over many months it has consistently performed in a reliable and predictable fashion.

Trials have shown that in the volume manufacture of multiple CPV cells per wafer, analysis can be done to isolate the causes of any processing variation thus helping in the prioritisation of continuous improvement work.

Techniques to further improve cell homogeneity have previously been reported by K.Heasman et al [4] by implementation of doping uniformity improvements. By these adjustments, a ±1% relative efficiency standard deviation has been demonstrated on CPV cells at all concentrations up to 100Sun.

Acknowledgements

The authors would like to thank Dr J. Korallus from Centrotherm GmbH for his helpful discussions of the Centrotherm systems. We would also like to thank Stephen Scott and the production team at NaREC Blyth PVTC for their assistance and co-operation.

References

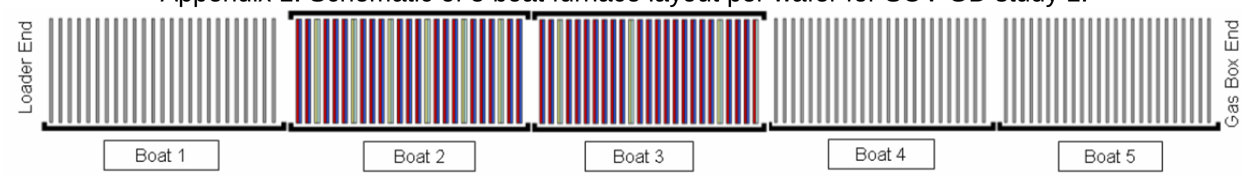
[1] K.Heasman et al., Proceedings of the CPV Optics and Power workshop, Marburg, 2007

[2] Dieter K Schroder, Semiconductor Material and Device Characterization, Wiley-IEEE, 2006

[3] Western Electric Company (1956), Statistical Quality Control handbook. (1 ed.), Indianapolis, Indiana: Western Electric Co.

[4] K.Heasman et al. Proceedings of the 22nd EU PVSEC (2007) 1511

Appendix 1. Schematic of 5 boat furnace layout per wafer for SOV GD study 1.



App1. 5 boat layout in Centrotherm furnace